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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,183	04/08/2004	Edward Grivna	16820P296	1767

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
WILLIAMS, HOWARD L	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,183	GRIVNA, EDWARD	
	Examiner	Art Unit	
	Howard L. Williams	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-16 and 18-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-16 and 18-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-16 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,177,482 to Cideciyan et al. Cideciyan discloses a RLL encoder operating on plural bytes in parallel pipeline to encode the eight bit source words to ten bit codewords (8B/10B). Cideciyan discloses evaluating a source character to determine the state value for that character to determine whether the state value will be either changed or not changed by the byte as a function of the previous state and the state indicator for the current source word (37, fig. 2) (col. 7, lines 39-54). Figure 2 shows the system for one byte whereas figures 6A and 6B show the pipeline arrangement for operating on four input bytes by placing multiple copies of single encoder in parallel. Cideciyan discloses comparing the previous state bit (15; fig. 2) with the current state indication (33; fig. 2) to determine whether the current source word will cause state toggling, i.e. the claimed "flip/hold" bit of the present application. The state toggling indicator is produced as a function of the current input byte held in input register (11; fig. 2). In the single word depiction of figure 2 the previous state and current state toggle indicator are compared in the exclusive OR gate (XOR 31; fig. 2) and fedback to a portion of the register 11 [S(N)]. In the pipelined or plural byte embodiment figure 5 the state value is passed to next stage of the plural byte encoder (36A; fig. 5; 36 fig. 4). After the last stage the output of the state comparison is fed back to the first stage (36D; fig. 5).

Cideciyan discloses in column 11 a modified encoder which seeks to mitigate any delay associated with the determination of the state transition bit by deriving it "in advance" (col. 11, line 27). This is seen as the equal to the now claimed intermediate coding.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,177,482 to Cideciyan et al. in view of U.S. Patent 5825309 A to Matsui et al.

or Millman Microelectronics Digital and Analog Circuits and Systems. Cideciyan discloses a RLL encoder operating on plural bytes in parallel pipeline to encode the eight bit source words to ten bit codewords (8B/10B). Cideciyan discloses evaluating a source character to determine the state value for that character to determine whether the state value will be either changed or not changed by the byte as a function of the previous state and the state indicator for the current source word (37, fig. 2) (col. 7, lines 39-54). Figure 2 shows the system for one byte whereas figures 6A and 6B show the pipeline arrangement for operating on four input bytes by placing multiple copies of single encoder in parallel. Cideciyan discloses comparing the previous state bit (15; fig. 2) with the current state indication (33; fig. 2) to determine whether the current source word will cause state toggling, i.e. the claimed "flip/hold" bit of the present application. The state toggling indicator is produced as a function of the current input byte held in input register (11; fig. 2). In the single word depiction of figure 2 the previous state and current state toggle indicator are compared in the exclusive OR gate (XOR 31; fig. 2) and fedback to a portion of the register 11 [S(N)]. In the pipelined or plural byte embodiment figure 5 the state value is passed to next stage of the plural byte encoder (36A; fig. 5; 36 fig. 4). After the last stage the output of the state comparison is fed back to the first stage (36D; fig. 5).

Cideciyan calls box 37 simply logic circuitry (col. 7, line 48) stating that it is for deriving the next state based on the data byte. In other words, it is evaluating the source character. The examiner considers that this logic block would have been obvious to implement either in logic gates or a look-up table. This is supported by Matsui et al. wherein it is recognized that look-up tables are logic circuitry (col. 8, line 34) and Millman who teaches on page 199 in the chapter dealing with combinational logic systems, i.e. logic, and look-up tables specifically that "Clearly, any calculation for which a truth table can be written may be implemented with a ROM"

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard L. Williams at telephone number (571) 272-1815.

Howard L. Williams

10/19/05
Voice: (571) 272-1815

Howard L. Williams
Primary Examiner
Art Unit 2819